**Vijaykrishnan Narayanan, Distinguished Professor**

Department of Computer Science and Engineering

Pennsylvania State University

354D Information Sciences and Technology Building

University Park, PA 16802

**Professional Preparation**

University of Madras Chennai, India Computer Science and Engr. B.E., 1993

University of South Florida Tampa, FL Computer Science and Engr. Ph.D., 1998

**Appointments**

2015- Distinguished Professor, Computer Science and Engineering and Electrical Engineering, Penn State University, University Park, PA

2007-current Professor, Computer Science and Engineering and Electrical Engineering,

Penn State University, University Park, PA

2003- 2007 Associate Professor, Computer Science and Engineering, Penn State Univ., University Park, PA

1998-2003 Assistant Professor, Computer Science and Engineering, Penn State Univ., University Park, PA

**Up to 5 Related Products**

1. [Nandhini Chandramoorthy](http://dblp.uni-trier.de/pers/hd/c/Chandramoorthy:Nandhini), [Giuseppe Tagliavini](http://dblp.uni-trier.de/pers/hd/t/Tagliavini:Giuseppe), [Kevin M. Irick](http://dblp.uni-trier.de/pers/hd/i/Irick:Kevin_M=), [Antonio Pullini](http://dblp.uni-trier.de/pers/hd/p/Pullini:Antonio), [Siddharth Advani](http://dblp.uni-trier.de/pers/hd/a/Advani:Siddharth), [Sulaiman Al Habsi](http://dblp.uni-trier.de/pers/hd/h/Habsi:Sulaiman_Al), [Matthew Cotter](http://dblp.uni-trier.de/pers/hd/c/Cotter:Matthew), [John Sampson](http://dblp.uni-trier.de/pers/hd/s/Sampson:John), Vijaykrishnan Narayanan, [Luca Benini](http://dblp.uni-trier.de/pers/hd/b/Benini:Luca): Exploring architectural heterogeneity in intelligent vision systems. [HPCA 2015](http://dblp.uni-trier.de/db/conf/hpca/hpca2015.html#ChandramoorthyT15): 1-12 (2015)
2. [Siddharth Advani](http://dblp.uni-trier.de/pers/hd/a/Advani:Siddharth), [Yasuki Tanabe](http://dblp.uni-trier.de/pers/hd/t/Tanabe:Yasuki), [Kevin M. Irick](http://dblp.uni-trier.de/pers/hd/i/Irick:Kevin_M=), [Jack Sampson](http://dblp.uni-trier.de/pers/hd/s/Sampson:Jack), Vijaykrishnan Narayanan:  
   A scalable architecture for multi-class visual object detection. [FPL 2015](http://dblp.uni-trier.de/db/conf/fpl/fpl2015.html#AdvaniTISN15): 1-8. 2015
3. V. Narayanan, [S. Datta](http://dblp.uni-trier.de/pers/hd/d/Datta:Suman), [G. Cauwenberghs](http://dblp.uni-trier.de/pers/hd/c/Cauwenberghs:Gert), [D. M. Chiarulli](http://dblp.uni-trier.de/pers/hd/c/Chiarulli:Donald_M=), [S. P. Levitan](http://dblp.uni-trier.de/pers/hd/l/Levitan:Steven_P=), [P. Wong](http://dblp.uni-trier.de/pers/hd/w/Wong:Philip). Video analytics using beyond CMOS devices. [DATE 2014](http://dblp.uni-trier.de/db/conf/date/date2014.html#NarayananDCCLW14): 1-5. (2014)
4. K. Ma, Zheng, Y., Li, S., Swaminathan, K., Li, X., Liu, Y., Sampson, J., Xie, Y., & Narayanan, V. (2015). Architecture exploration for ambient energy harvesting nonvolatile processors. 21st IEEE International Symposium on High Performance Computer Architecture, HPCA 2015, Burlingame, CA. pp. 526–537. **Best Paper Award**
5. [M. J. Cotter](http://dblp.uni-trier.de/pers/hd/c/Cotter:Matthew_J=), [Y. Fang](http://dblp.uni-trier.de/pers/hd/f/Fang:Yan), [S. P. Levitan](http://dblp.uni-trier.de/pers/hd/l/Levitan:Steven_P=), [D. M. Chiarulli](http://dblp.uni-trier.de/pers/hd/c/Chiarulli:Donald_M=), V. Narayanan. Computational Architectures Based on Coupled Oscillators. [ISVLSI 2014](http://dblp.uni-trier.de/db/conf/isvlsi/isvlsi2014.html#CotterFLCN14): 130-135.

**Up to 5 Other Products**

1. [J. P. Sustersic](http://dblp.uni-trier.de/pers/hd/s/Sustersic:John_P=), [B. Wyble](http://dblp.uni-trier.de/pers/hd/w/Wyble:Brad), [S. Advani](http://dblp.uni-trier.de/pers/hd/a/Advani:Siddharth), V. Narayanan. Towards a unified multiresolution vision model for autonomous ground robots. [Robotics and Autonomous Systems 75](http://dblp.uni-trier.de/db/journals/ras/ras75.html#SustersicWAN16):221-232. (2016)
2. V. Saripalli, S. Datta, and V. Narayanan. Ultra Low Power Signal Processing Architectures enabling Next-Generation BioSensing and Biomimetic System. Proceedings of the IEEE Biomedical Circuits and Systems Conference. (August 2008)
3. D. Duarte, N. Vijaykrishnan, M. J. Irwin. A Clock Power Model to Evaluate Impact of Architectural and Technology Optimizations. *IEEE Transactions on VLSI*, 10(6):844-855. (December 2002) **IEEE Circuit** **and Systems Transactions on VLSI Best Paper Award**
4. H. Moon, K. Irick, V. Narayanan, R. Sharma, N. Jung. April 24, 2012, Apparatus and method for measuring audience data from image stream using dynamically-configurable hardware architecture, U.S. Patent 8165386.
5. N. Shukla, A. Parihar, M. Cotter, M. Barth, X. Li, N. Chandramoorthy, D. G. Schlom, V. Narayanan, A. Raychowdhury and S. Datta, “Pairwise coupled hybrid vanadium dioxide-MOSFET (HVFET) oscillators for non-boolean associative computing,” Proceedings of the IEEE International Electron Devices Meeting (IEDM 2014).

**Synergistic Activities**

*Editorial Activities*

* Editor-in-Chief, IEEE Transactions on CAD, 2014-current

*Technical Leadership*

* Chair, ACM Special Interest Group on Design Automation, August 2015-Current
* Invited Participant, 2015 White House Brain Conference

# *Educational/Outreach Activities*

# Hosted a high school teacher in summer 2015 as part of a NSF RET program for incorporation of smart cameras and organized a workshop for a dozen high school teachers.

* Supervised two high school women students in summer 2015 and helped them develop an application based on combining sensor information for smart health application
* Demonstrated a Visual Shopping Assistance Vision System at the Coalition of National Science Funding Exhibition in Capitol Hill, Washington D.C.